IN THE CLAIMS:

Please amend the claims as follows.

1. (Currently Amended) A method for controlling transitions between a first and a second clock frequency ~~signal~~ in first and second components electrically coupled together and in communication with one another, the method comprising:

configuring a register in each of the first and second components with an indication of the second clock frequency to initiate the transitions between the first and the second clock frequency;

asserting a freeze signal to cause communications between the first and second components to cease;

receiving a freeze acknowledge signal from each of the first and second components indicating that communications there between have ceased; and

delivering a change signal to the first and second components to cause each of the components to generate a clock signal consistent with the second clock frequency indicated by the corresponding register to switch between the first and the second clock frequency ~~signals~~.

2. (Currently Amended) An apparatus for controlling transitions between a first and a second clock frequency ~~signal~~ in first and second components electrically coupled together and in communication with one another, the method comprising:

means for configuring a register in each of the first and second components with an indication of the second clock frequency to initiate the transitions between the first and the second clock frequency;

means for asserting a freeze signal to cause communications between the first and second components to cease;

means for receiving a freeze acknowledge signal from each of the first and second components indicating that communications there between have ceased; and

means for delivering a change signal to the first and second components to cause each of the components to generate a clock signal consistent with the second clock frequency indicated by the corresponding register to switch between the first and the second clock frequency ~~signals~~.

3. (Currently Amended) An apparatus, for controlling transitions between a first and a second clock frequency ~~signal~~, comprising:

a first component ~~capable of receiving a freeze signal and delivering an acknowledge signal after communications therefrom have been ceased~~;

a second component ~~capable of receiving the freeze signal and delivering an acknowledge signal after communications therefrom have been ceased~~; ~~and~~

a register comprised in each of the first and second components, wherein each of the registers are configured with an indication of the second clock frequency to initiate the transitions between the first and the second clock frequency; and

a controller ~~capable of delivering~~ configured to deliver the freeze signal requesting that the first and second components cease communications therebetween [[,]] ~~and transitioning between the first and second clock signals~~ ;

wherein the first and second components are each configured to receive the freeze signal and to deliver the corresponding acknowledge signal after communications between the first component and the second component have been ceased;

wherein, in response to receiving the acknowledge signals from the first and second components, the controller is further configured to deliver a change signal to cause each of the components to generate a clock signal consistent with the second clock frequency indicated by the corresponding register to switch between the first and the second clock frequency.

4. (New) The method of claim 1, further comprising deasserting the freeze signal after the generated second clock frequency signal stabilizes, to resume the communications between the first and second components.

5. (New) The method of claim 1, wherein said configuring the register in each of the first and second components with the indication of the second clock frequency comprises writing data that is indicative of the second clock frequency into each of the registers.

6. (New) The method of claim 1, wherein the switch between the first and the second clock frequency changes the operating power mode of the components from a normal power operating mode to a reduced power operating mode.

7. (New) The method of claim 1, wherein, in response to receiving the change signal, the second clock frequency signal is generated by each of the components based on the contents of the corresponding register to switch between the first and the second clock frequency.

8. (New) The apparatus of claim 3, wherein the controller is further configured to deassert the freeze signal after the generated second clock frequency signal stabilizes, to resume the communications between the first and second components.

9. (New) The apparatus of claim 3, wherein the controller is further configured to write data that is indicative of the second clock frequency into each of the registers.

10. (New) The apparatus of claim 3, wherein, in response to receiving the change signal from the controller, the second clock frequency signal is generated by each of the components based on the contents of the corresponding register to switch between the first and the second clock frequency.

11. (New) The apparatus of claim 3, wherein the first and second components are configured as dynamic memory devices, and wherein the first and second components are operable to enter a self refresh mode during transitions between the first and the second clock frequency to prevent corruption or loss of the data stored therein.

12. (New) The apparatus of claim 11, wherein the first and the second components are configured as dynamic memory devices, and wherein the first and second components are operable to enter the self refresh mode after the controller receives the freeze acknowledge signals and before the controller delivers the change signal.